REMARKS

Claims 1-27 currently are pending, of which claims 5-12 and 17-25 are withdrawn from consideration by the Examiner as being drawn to non-elected inventions.

On page 2 of the Office Action, the Examiner requires amending the title to more clearly indicate the invention to which the claims are directed. As indicated above, the title of the invention is amended. It is respectfully submitted that the amended invention title fully complies with the 37 C.F.R. § 1.72.

Pages 2-3 of the Action includes a rejection of claims 16, 26 and 27 under 35 U.S.C. § 112, second paragraph, as being indefinite. Specifically, the Examiner objected to the claimed terms "to be" and "to be further" recited in claim 16 for allegedly not reciting positive claimed structure. While Applicants disagree that this language renders the claims indefinite, especially when reading the claim in light of the specification, or that any law or rule bars patentability when these terms are recited in claims, claim 16 has been changed to remove the language objected to in the Action.

Additionally, the Examiner asserts the recitation "a fourth bonding wire electrically connecting said second bonding wire with said second electrode pad," is unclear and confusing. In response, claim 16 is amended to improve readability and address minor informalities. It is respectfully submitted that amended claim 16 fully complies with Section 112, second paragraph. Accordingly, Applicants request the Examiner to withdraw this rejection.

Pages 3-6 of the Office Action include a rejection of claims 1-4, 13-16, 26 and 27 under 35 U.S.C. § 102 as allegedly being anticipated by Brooks (U.S. Patent Application Publication No. US 2003/0153122 A1). Insofar as the Office may consider this rejection to apply to the amended claims, Applicants respectfully traverse.

Starting with amended claim 1, it is respectfully submitted that the Brooks publication does not describe the claimed feature of a semiconductor chip with a rectangular main surface and a functional element, as recited in the context of the other claimed features. In setting forth the rejection of claim 1, Examiner asserts that the Brooks publication describes a semiconductor chip 206. However, Brooks is silent as to whether the silicon interposer 206, which is described in detail in paragraphs 0025-0026, includes a functional element as claimed. Moreover, claim 1 recites *inter alia* "a plurality of first interconnections, wherein each first interconnection is connected between one of the main electrode pads and one of the first electrode pads, and a plurality of second interconnections, wherein each second

interconnection is connected between one of the main electrode pads and one of the second electrode pads." In connection with these features, the Examiner relies upon the bond pads 108 shown in prior art Figure 1 for allegedly showing a second interconnection. However, the description of the Figure 1 arrangement in paragraph 0005 of the Brooks publication does not mention, nor do Figures 1-4 relied upon show that "each second interconnection is connected between one of the main electrode pads and one of the second electrode pads," as claimed.

Moreover, the Brooks publication does not show the claimed "first distance" and "second distance that is longer than the first distance," in connection with respective locations of first and second electrode pad groups, as recited in amended claim 1. Support for these features is found, for example, in Figure 1A, and the description thereof starting at page 12 of the specification.

Hence, the Brooks publication fails to describe a number of features set forth in independent claim 1. Accordingly the rejection of claim 1 should be withdrawn.

Claim 16 likewise recites subject matter setting forth patentable distinctions. For instance, claim 16 recites *inter alia* "a first semiconductor chip having a rectangular main surface and a functional element," "a second semiconductor chip having the same configuration of the first semiconductor chip and mounted on said first semiconductor chip laminated in said main surface." As pointed out above, the Brooks publication does not mention that the interposer comprises a semiconductor chip and that such a chip includes a functional element as claimed. Additionally, the claim 16 combination recites "a first electrode pad group composed of a plurality of first electrode pads which is located between said first side and said main electrode pad group with a first distance, wherein said plurality of first electrode pads is arranged on said main surface along said first side; a second electrode pad group composed of a plurality of second electrode pads which is located between said second side and said main electrode group with a second distance which is longer than said first distance, wherein plurality of second electrode pads is arranged on said main surface along said second side," and "a plurality of first interconnections, wherein each first interconnection is connected between one of the main electrode pads and one of the first electrode pads; and a plurality of second interconnections, wherein each second interconnection is connected between one of the main electrode pads and one of the second electrode pads." In contrast, the Brooks publication does not appear to describe or show any interconnection connecting between the bond pads 108 to the bond pads 212, 402, much less

PAGE 19/21 * RCVD AT 2/3/2006 10:36:23 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID:866 741 0075 * DURATION (mm-ss):05-56

the claimed first and second distances.

Hence, for reasons analogous to those given above, the rejection of claim 16 should be withdrawn.

The Office also rejects claims 1-4, 13-16, 26 and 27 under 35 U.S.C. § 103 as allegedly being obvious over Sadao (Japanese Patent Publication No. 2001-007278). This rejection is respectfully traversed, as the Sadao publication fails to teach or suggest a number of the features set forth in the combinations of features set forth in amended claim 1 and 16.

With respect to claim 1, the Examiner asserts, at page 7 of the Action, that the Sadao publication shows a semiconductor chip 2 as including "a main electrode pad group (second row of 13 on 2) ...," "a first electrode pad group (second row of 13 on 2) ...," and "a second electrode pad group (third row of 12 on 2) ...." It is respectfully submitted, however, that the bonding pads 12 and 13 of the Sadao device are parts of a wiring sheet (shown as item 9), which is used as an interposer for chips of different size or having different positions of bonding pads (see, Figure 1, the "Problems to be Solved" section of the English language abstract, and the first three lines of the "Solution" section of the abstract). Furthermore, it is neither described nor suggested in the English language abstract of Sadao that the wiring sheet is a semiconductor chip having a functional element as claimed.

The Sadao publication also fails to teach or suggest the semiconductor device as recited in claim 16, which comprises a plurality of semiconductor chips, each having a functional element, and piled on a substrate. By contrast, Sadao discloses a *wiring sheet* used as an interposer between chips. As pointed out above, there is no suggestion in Sadao that the wiring sheet interposer comprise a semiconductor chip having functional elements.

Furthermore, Applicants respectfully disagree with the Examiner's allegation concerning the Sadao document teaching the semiconductor chip 2 comprising a main pad group and a second electrode pad group. To the contrary, the Sadao publication explicitly describes that bonding pad groups 12 and 13 are formed on the wiring sheet interposer, which appears to be bonded between the semiconductor chips 2 and 3. Indeed, the stated purpose in Sadao for the *wiring sheet* interposer is to connect chips of various sizes or bonding pad arrangements to a package board. In contrast, the present invention recited in claim 16 provides at least two semiconductor chips, each including *inter alia* a main electrode pad group, a first electrode pad group, and a second electrode pad group, as claimed., which is a significant departure from chip arrangements such as described in Sadao. For example, the present invention facilitates forming thinner devices than those such as Sadao's, which utilize

PAGE 20/21 * RCVD AT 2/3/2006 10:36:23 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID:866 741 0075 * DURATION (mm-ss):05-56

wiring sheet interposers in stacked chip arrangements.

For at least these reasons, it is respectfully submitted that the present invention as set forth in independent claims 1 and 16 would not have been obvious in view of the Sadao patent publication.

The remaining claims 2-4, 13-15, 26 and 27 depend from one of allowable independent claims 1 and 16, and therefore are themselves allowable. Furthermore, the dependent claims recite combinations including additional features not described in the Brooks publication, and not taught or suggested in the Sadao publication.

On pages 6-7, the Examiner cites caselaw regarding integration of multiple pieces into one piece. However, it is not clear how the cited caselaw relates to the applied prior art. For instance, there is no statement concerning what the prior art is missing with respect to the claimed features. If the Examiner maintains this rejection in the next communication to Applicant, it is respectfully requested that he provide further explanation pointing out the shortcomings of the Sadao publication and why the cited caselaw applies to features missing in the Sadao patent.

All of the objections and rejections raised in the Office Action having been addressed above, the present application is believed in condition for allowance. Prompt notification of the same is earnestly sought. Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,

John F. Guay
Registration No. 47,248

Nixon Peabody LLP
401 9th Street N.W.
Suite 900
Washington, D.C. 20004
(202) 585-8000

PAGE 21/21 * RCVD AT 2/3/2006 10:36:23 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID:866 741 0075 * DURATION (mm-ss):05-56